Guest Lecture on VLSI Desgin and its Future direction

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By

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When we are going down the technology, the scaling of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) predicted by the ITRS involves very important leakage current which seems to be not easily manageable with conventional MOS architectures. An alternative solution consists in employing field-effect transistors on silicon on insulator substrate (SOI). This solution exists since a long time but is not widely used in an industrial context. However, the main advantage of using ultra thin silicon is to guarantee an excellent electrostatic channel control by the gate, thus reducing the short channel effects and consequently the leakage currents even for channel length lower than 20 nm. When a second gate is introduced under the silicon film in the buried oxide, this

electrostatic control is drastically improved. This last category of device architecture, called double gate MOSFET (DGMOS), offers serious advantages in term of electrical performance, In addition, when both gates can be independently driven, this device architecture opens new perspectives in term of innovative circuit design.
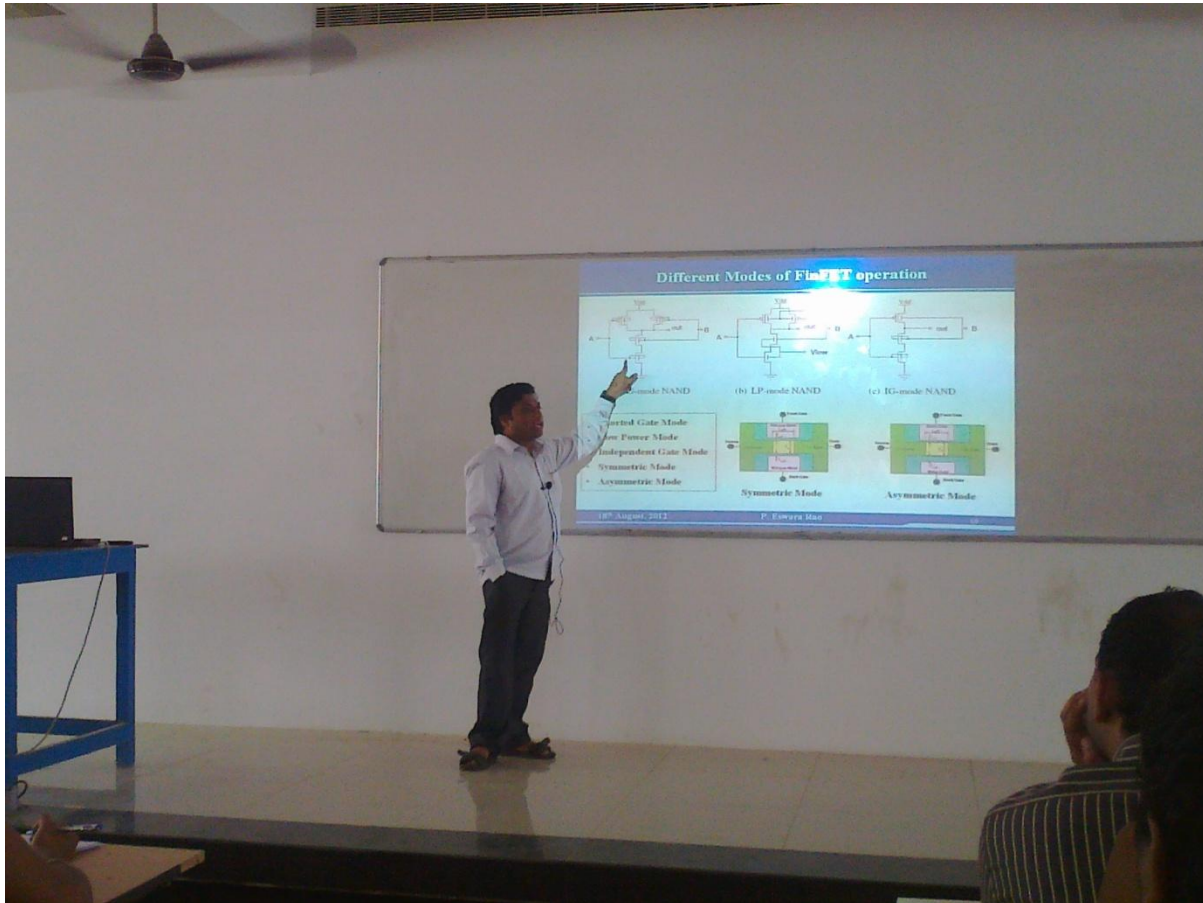
To take advantage of the double gate MOSFET (DGMOS) architecture with independent driven gates, designers need compact models to imagine new circuits. Criteria of a good compact model are simple equations, short computing time, few fitting parameters and predictive. From a circuit design point of view, the computing time is a very significant parameter. So this talk starts with the description of the double gate CMOS technology, from the MOS transistor modelling using threshold voltage based approach. And then an in-depth analysis of Analog design and SRAM design using Independently Driven Double-Gate technology is by presenting several cell topologies. In conventional transistors the drain current is controlled by a 'single' gate voltage, whereas in DG structures two independent gates can be available to adjust the drain current.

This double controllability offers a new degree of freedom, which enables novel architectures.

Author Profile

Work Experience:

- ❖ Presently working as Sr Staff Engineer in Technology and Hardware Development of IBM Bangalore,
- ❖ Adjunct Professor at IIIT Bangalore.

Previously

- ❖ Worked as Assistant Professor at NIT Nagpur from Sept 2009 to October 2011.
- ❖ As Design Engineer at Elpida Memory from August 2007 to August 2009.
- ❖ Member of IBM-IIT Bombay Project Collaboration

❖ Work Experince on Analog, Memory and FinFET Circuit Designs

Education:

❖ Registered for PhD from (NIT Nagpur and IIT Bombay)
❖ M.Tech (VLSI) from NIT Nagpur- 2007
❖ B.Tech (ECE) from JNTU Hyderabad- 2005

Publications/Projects

❖ Granted with Two Patents.
❖ Published 6 papers in International Conferences
❖ Published 7 papers in National Level Conferences

Professional Activities

❖ Invited Speaker at National Level Workshop at NIT Nagpur organized by NIT Nagpur and IIT Bombay.
❖ Guest talk on FinFET Technology to Analog Design at SASTRA University and IIT Indore.
❖ Reviewer for ISTL Technical Conference at IBM
❖ Reviewer for 25th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)-2012.
❖ Reviewer for IEEE Conference on Electrical, Electronic and Computer Science (SCEECS)-2010 at NIT Bhopal.
❖ Member of the Expert Panel at RV VLSI Bangalore

Achievements:

❖ Got IBM Innovation Excellence Award for multiple ideas,papers and disclosures.
❖ Got IBM Best Collaborator Award for collaboration with SRDC ,China and Japan Teams.
❖ Got Best Mentor Award from TI for guiding an award winning project in TI Analog Desgin Contest-2011.
❖ Played a Key role in setting up TI Analog Design Research Lab at NIT Nagpur Got the Best Project Award from Cadence Design Contest- 2007 for the M.Tech project on Bulk Driven OPAMP.

Academic Experience:

- ❖ Taught Low Pwer CMOS Design and CMOS Analog Circuit Design couple of times.
- ❖ Was the Exam Coordinator from July 2010 to July 2011 at NIT Nagpur.
- ❖ Was the Coordinator for IEEE Technical Activies/Tech Talks at NITNagpur