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Ref: KLEF/RO/ECE/CIRCULAR **Date: 13-03-2022**

CIRCULAR

Sub: Organizing event "Workshop" for the students of Electronics and Communication Engineering, of Vaddeswaram Campus of KLEF – Reg.

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This is to inform that the Department of Electronics and Communication Engineering, KLEF, is Organizing a "Workshop on Semi Custom Design Flow" for the students of Electronics and communication Engineering, Vaddeswaram Campus of KLEF on, 16-03-2022, as details below:

Event Name: "Workshop"
Date: 16-03-2022
Venue: R-106

All the students of ECE, are invited to attend this program.
Dy-HOD's & Year coordinators are requested to bring this information to the attention of all ECE students and encourage them to participate in this program.

HOD/ECE
Dr M. Suman
Dr. M. SUMAN
Professor & Head
Department of ECE
K L E F
Green Fields, Vaddeswaram
Guntur Dist., A.P. PIN: 522 502

To
All ECE Students,
All ECE Faculty,
Principal.

Koneru Lakshmaiah Education Foundation
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A Three-Day Workshop On "Semi Custom Design Flow".

By

Always@VLSI

Department Of ECE

Name of the event: Semi Custom Design Flow

Dates: 16-03-2022

Venue: R106

No. of students participated: 80

Objective of the event:

In the realm of technological innovation and chip design, a transformative educational experience unfolded during the "Semi Custom Design Flow" workshop. Held over four days, this event aimed to illuminate the world of chip design to students and elucidate potential job roles associated with each design step. With a focus on Cadence software and its role in the industry, students were given a comprehensive understanding of the intricate VLSI design process, from RTL to GDS.

Description of the event:

Day 1: Orientation and VLSI Design Overview

The workshop kicked off with an informative orientation session, setting the stage for an intensive exploration of VLSI (Very Large Scale Integration) design. Students were provided with an overview of VLSI design, encompassing the essential concepts and processes involved. This introductory day aimed to establish a solid foundation and a common understanding of the VLSI design flow.

Day 2: Introduction to Cadence Suite Tools and RTL Design

On the second day, students were introduced to key Cadence suite tools, including Incisive, Genus, and Innovus. The focus was on understanding the role and significance of these tools in the chip design process. A substantial portion of the day was dedicated to RTL (Register Transfer Level) design, where students were guided through the process of creating their RTL designs. Practical applications and hands-on exercises allowed the students to gain firsthand experience in RTL design.

Day 3: Simulations and Synthesis

The third day immersed the students in simulations and synthesis, crucial components of the VLSI design flow. They were provided with in-depth knowledge of simulation processes using Cadence Incisive, emphasizing formal verification and the importance of constraints. Following this, students ventured into the synthesis phase, understanding its role in transforming RTL designs into optimized netlists. Constraints and their role in synthesis were underscored, providing a comprehensive understanding of this vital stage in chip design.

Day 4: Physical Design

The fourth and final day delved into the critical phase of physical design. Students were introduced to the Innovus tool, where they learned about floorplanning, power planning, placement, clock tree synthesis, and routing. The process involved mapping the design to the foundry using technology and physical libraries, culminating in the generation of GDS (Graphic Data System) files, which are essential for fabrication. Throughout this day, students actively engaged in the design optimization process using Engineering Change Orders (ECO) and were guided in generating reports at each step, providing them with a comprehensive understanding of the physical design process.

This structured four-day workshop was designed to equip students with the knowledge and practical skills essential for a career in chip design. The progressive learning approach, starting from an overview and gradually delving into tool introduction, RTL design, simulations, synthesis, and physical design, ensured a thorough understanding of the VLSI design flow. The hands-on experience provided a tangible grasp of the concepts, preparing the students for a successful journey in the world of chip design.

Outcome of the event:

Inspired by the Semi Custom Design Flow workshop, the participating students undergo a profound transformation in their perception and engagement with the realm of chip design.

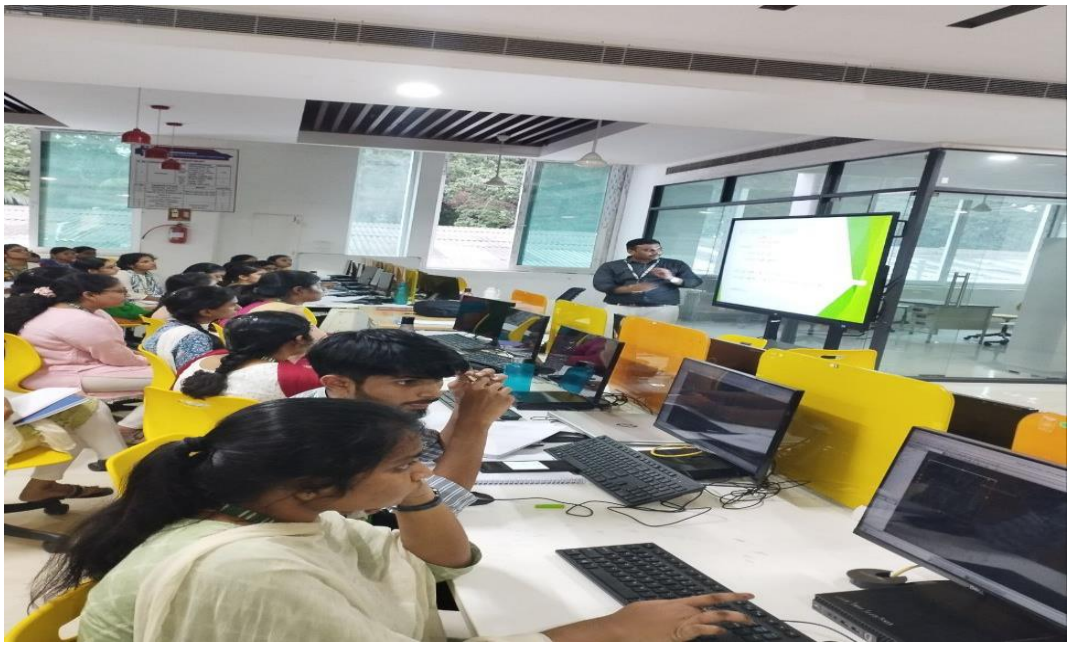
Equipped with enriched knowledge and hands-on experiences, they emerge as proficient contributors in the domain of VLSI design.

These learners, now armed with a thorough understanding of the design process intricacies and industry-standard tools, step into their professional endeavors with a newfound sense of purpose. The practical exposure and collaborative exercises during the workshop have refined their problem-solving capabilities and technical expertise, positioning them as valuable resources in the ever-evolving landscape of chip design.

The networking opportunities provided during the workshop have not only expanded their professional networks but have also laid the groundwork for potential partnerships and innovative projects. Fueled by the shared enthusiasm sparked at the workshop, these students become proactive contributors to the continuous advancement of chip design technology, whether through research, entrepreneurship, or industry involvement.

As they venture into the professional arena, these individuals transcend being merely graduates; they are pioneers prepared to navigate the challenges and seize the opportunities presented by chip design. The impact of the workshop extends beyond mere knowledge acquisition, shaping a cohort of professionals who are not mere spectators but active drivers of the transformative journey toward a future defined by innovative chip designs and advancements in technology.

photos of the event:



Faculty explaining the semi custom design flow

Student mentors guiding the students in hands on session

List of Participated Students

S.No	Name	ID Number	Branch	SIGNATURE
1.	190040605	SIMHADRI DEEPIKA REDDY	ECE	
2.	190040603	SOMEPALLI JYOTHI PRAKASH	ECE	
3.	190040593	AISWARYA S T P	ECE	
4.	190040591	YERUVA NITESH KUMAR REDDY	ECE	
5.	190040589	YERRAGURAVAGARI PUJITHA	ECE	
6.	190040587	YEMINENI CHAKRAVARTHI	ECE	
7.	190040585	YELLAPRAGADA SRI VENU KAMAL	ECE	
8.	190040584	YASHWANT VENKATA SAI PULI	ECE	
9.	190040582	YARRAGOLLA HARSHAVARDHAN	ECE	
10.	190040581	YARAGUTI MAHENDRA REDDY	ECE	
11.	190040563	PARA VENKATA VINOD KUMAR	ECE	
12.	190040545	VANGA SATVIK REDDY	ECE	
13.	190040537	VADREVU RUTHVIK SHARMA	ECE	
14.	190040534	URLANA YASWANTH	ECE	
15.	190040525	TUMMALA RASATHVIKA	ECE	
16.	190040524	TUMMALA KARTHIK	ECE	
17.	190040522	TORATI AJAY CHANDRA	ECE	
18.	190040513	TARIGONDA JAHNAVI	ECE	
19.	190040506	SYAMALA NAGA KOTI REDDY	ECE	
20.	190040503	SUREDDY DINESH REDDY	ECE	
21.	190040501	SURAGAM GNANENDRA	ECE	
22.	190040495	SUBRAMANYAM YADAVILLI	ECE	
23.	190040483	SISTLA SATHWIC SANJAY	ECE	
24.	190040474	SHAIK MOHAMMED KHAALID	ECE	
25.	190040470	SHAIK JOHN ASIF	ECE	
26.	190040468	SHAIK GOUSE RABBANI	ECE	
27.	190040462	SHAIK ABDUL VADOOD	ECE	
28.	190040460	SHAIK HAMEED BASHA	ECE	
29.	190040453	SANGETA SATYA SWETHA DEVI	MEC	
30.	190040449	SAMIRAJU SAI BHANUTEJA	ECE	
31.	190040438	REVU CHANIKYA RAJU	ECE	
32.	190040415	PARASARAM SUSEEL KOUSIC	ECE	
33.	190040411	POTHANI PRABHUKIRAN	ECE	
34.	190040410	PONNADI RAJENDRA	ECE	
35.	190040404	POGAKU DIVYASREE	ECE	
36.	190040377	P AKHIL REDDY	ECE	
37.	190040372	NUKALA AKSHAY KUMAR	ECE	
38.	190040367	NI HARSHA VARDHAN REDDY	ECE	
39.	190040357	NADAKUDITI TARUN CHANDU	ECE	
40.	190040354	MUTNURU VENKATA ABHISHEK	ECE	
41.	190040605	SIMHADRI DEEPIKA REDDY	ECE	
42.	190040603	SOMEPALLI JYOTHI PRAKASH	ECE	
43.	190040593	AISWARYA S T P	ECE	
44.	190040591	YERUVA NITESH KUMAR REDDY	ECE	
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In charge
Always@VLSI Technical Club
Mr S. Vamsee Krishna

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