CERTIFICATE COURSE ON XILINX & CADENCE

Name of the Certificate Course: **XILINX EDA Tools**

Eligibility : ECE/ECM/EEE/CSE

Course Instructors : 1. Mr. T. Praveen Blessington
2. Mr. B. Murali Krishna

Software Requirements : XILINX Tool

Course Starting Date :

Evaluation : 1st Internal Lab Exam 20 Marks
2nd Internal Lab Exam 20 Marks
External Lab Exam 60 Marks
Total **100 Marks**

Course Objectives

The course is designed for B.Tech ECE students to introduce how the write a Verilog HDL code for the digital system. To expose the complexities and design methodologies of advanced Digital IC design technologies. The student can able to do academic & research projects by having the expertise with the Verilog. Verilog synthesis tools can create logic circuit structures from their behavioral description to design, simulate and synthesize anything from a simple circuit to a complete System-on-chip module.

1. Lesson Plan

No. of Theory Classes	Topics to be covered
1.	Introduction to Verilog
2.	Verilog Module Declaration, Nets, Variables, Constants
3.	Modeling at Data- Flow
4.	Modeling at Behavioral Design-1
5.	Modeling at Behavioral Design-1I
6.	Modeling at Structural
7.	Functions, Tasks & User Defined Primitives
8.	System Tasks, Functions & Compiler Directives
9.	Introduction to Xilinx ISE

10.	Design Flow Process
11.	Synthesis
12.	Implementation
13.	CPLDs
14.	FPGAs
15.	Verification on Target Devices.

2. Experiments List:

S.No	List of Experiments
1.	Design of Logic Gates
2.	Design of Decoders, Encoders
3.	Design of Priority Encoder
4.	Design of Multiplexers, Demultiplexers
5.	Design of Adders, Subtractors
6.	Design of Ripple Carry Adder, Carry Look Ahead Adder
7.	Design of Latches, Flip-Flops
8.	Design of Registers
9.	Design of Synchronous Counters
10.	Design of Asynchronous Counters
11.	Design of State Machines
12.	Design of ALU

3. Learning objectives:

Lecture No	Learning Objective	Topics to be Covered	Text Book / Reference
1	Importance of Verilog	Introduction to Verilog	T2/T3
2	Definitions for important terms in Verilog	Verilog Module declaration, Nets, Variables, Constants	T2/T3
3	Boolean expression-concurrency statements	Modeling at Data- Flow	T2/T3
4	Case statements-sequential statements	Modeling at Behavioral Design-1	T2/T3
5	If statements, loop, for & while statements	Modeling at Behavioral Design-II	T2/T3

6	Component instantiations	Modeling at Structural	T2/T3
7	Arguments, return statements	Functions, Tasks & User Defined Primitives	T2/T3
8	Behavioral syntax	System Tasks, Functions & Compiler Directives	T2/T3
9	Cad tools introduction	Introduction to Xilinx ISE	T1
10	Hierarchy to fabrication	Design Flow Process	T1
11	Generating net lists	Synthesis	T1
12	Pin assign, floor planning, routing	Implementation	T1
13	PLD kits downloading	CPLDs	T1
14	Gate-array kits downloading	FPGAs	T1
15	Checking the outputs by giving their subsequent inputs	Verification on Target Devices.	T1

References Manuals and Text books:

1. XILINX User Guide
2. Verilog Primer by J. Bhaskar
3. Verilog Digital Design Synthesis by Samir Palnitkar

Cadence Certification Program

Course content:

- **Introduction to Linux, Scripting, Editing**
- **Analog Course**

  Analog IC Design

  Virtuoso Schematic Editor

  Virtuoso Analog Design Environment
- **Digital Course**

  Introduction to Digital IC Design

  Verilog Language

  Encounter RTL Compiler

  Basic STA

  EDI- Floor planning, Physical Synthesis, Place and Route

Course Duration:

One Semester (4 hours /week)

Course Conducted:

2012-2013 first semester for M Tech (VLSI,CR) 19 students

2013-2014 first semester for M Tech (VLSI,CR) [ongoing]. 31 students